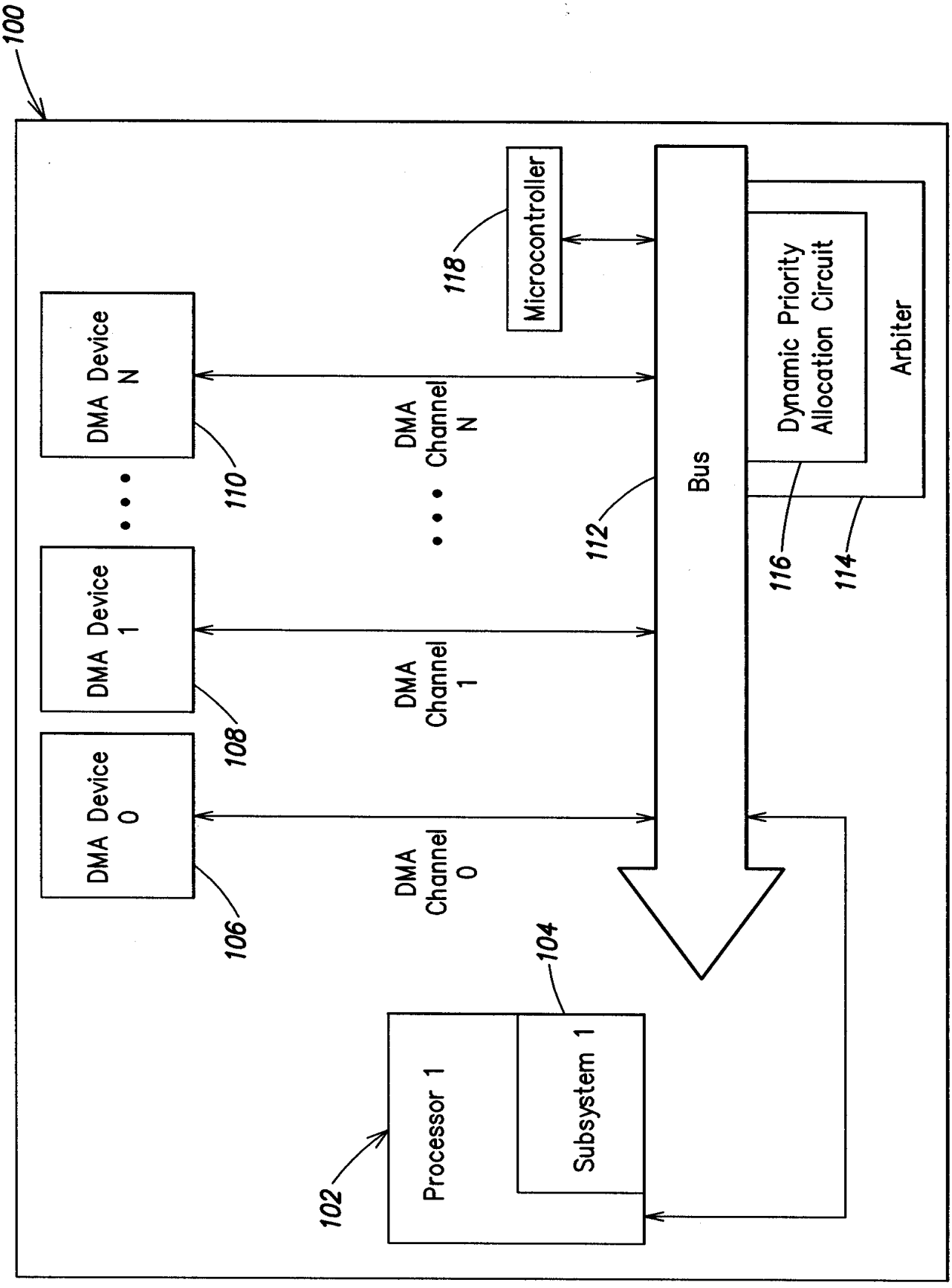
100
DMA Device N
DMA Device 1
DMA Device 0
110
108
106
DMA Channel N
DMA Channel 1
DMA Channel 0
118
Microcontroller
112
Bus
Dynamic Priority Allocation Circuit
Arbiter
116
114
104
Subsystem 1
Processor 1
102

FIG. 1

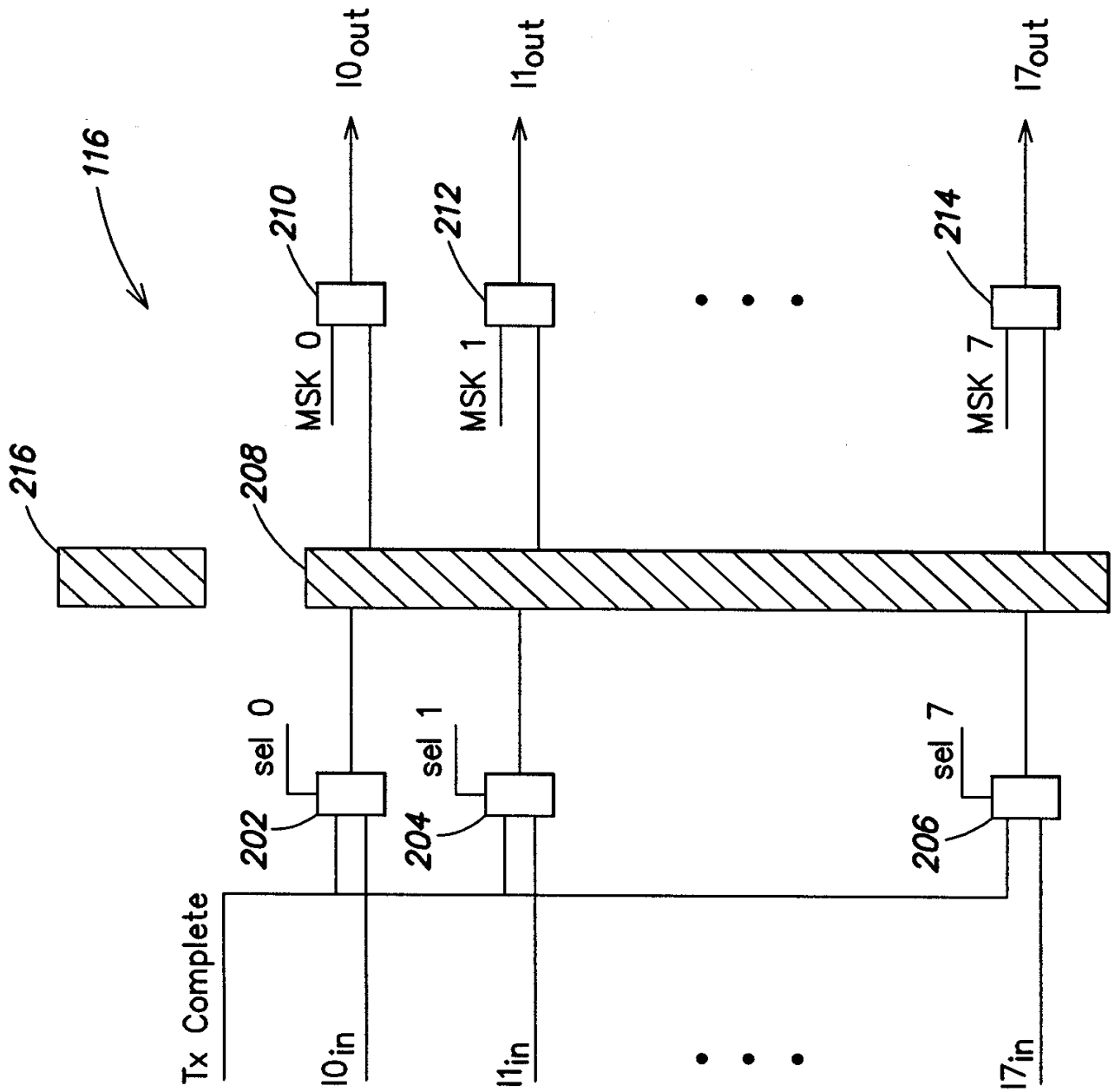
116
216
208
210
212
214
MSK 0
MSK 1
MSK 7
$I0_{out}$
$I1_{out}$
$I7_{out}$
sel 0
sel 1
sel 7
202
204
206
Tx Complete
$I0_{in}$
$I1_{in}$
$I7_{in}$

FIG. 2

300

Processor/DMA	Priority
CPU	0
Slave	1
CPU	2
DMA Channel 0	3
CPU	4
DMA Channel 1	5
CPU	6
DMA Channel 2	7
CPU	8
DMA Channel 3	9
CPU	10
DMA Channel 4	11
CPU	12
DMA Channel 5	13
CPU	14
DMA Channel 6	15
CPU	16
DMA Channel 7	17

← RST Value

FIG. 3

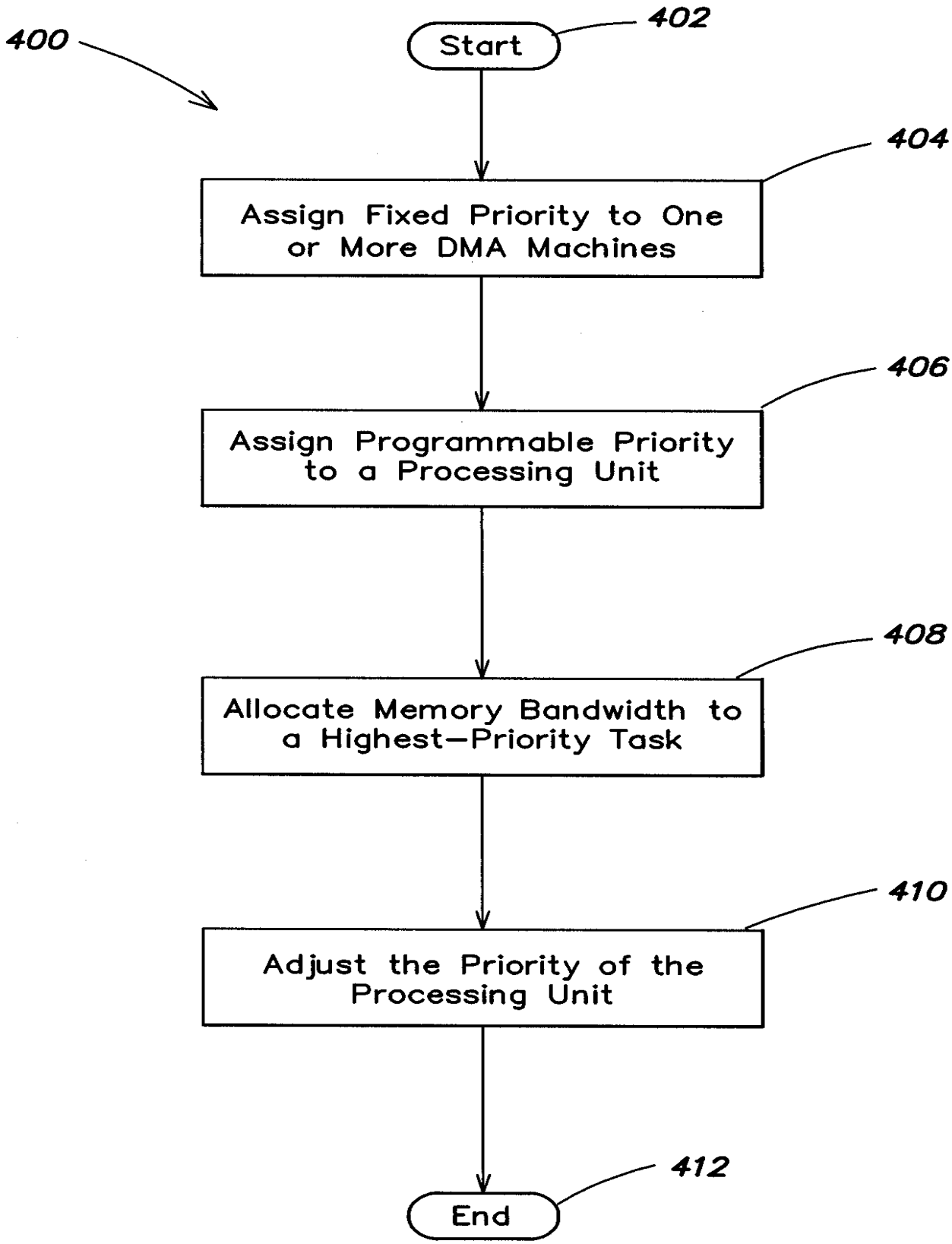
400
Start
402
Assign Fixed Priority to One or More DMA Machines
404
Assign Programmable Priority to a Processing Unit
406
Allocate Memory Bandwidth to a Highest–Priority Task
408
Adjust the Priority of the Processing Unit
410
End
412

FIG. 4

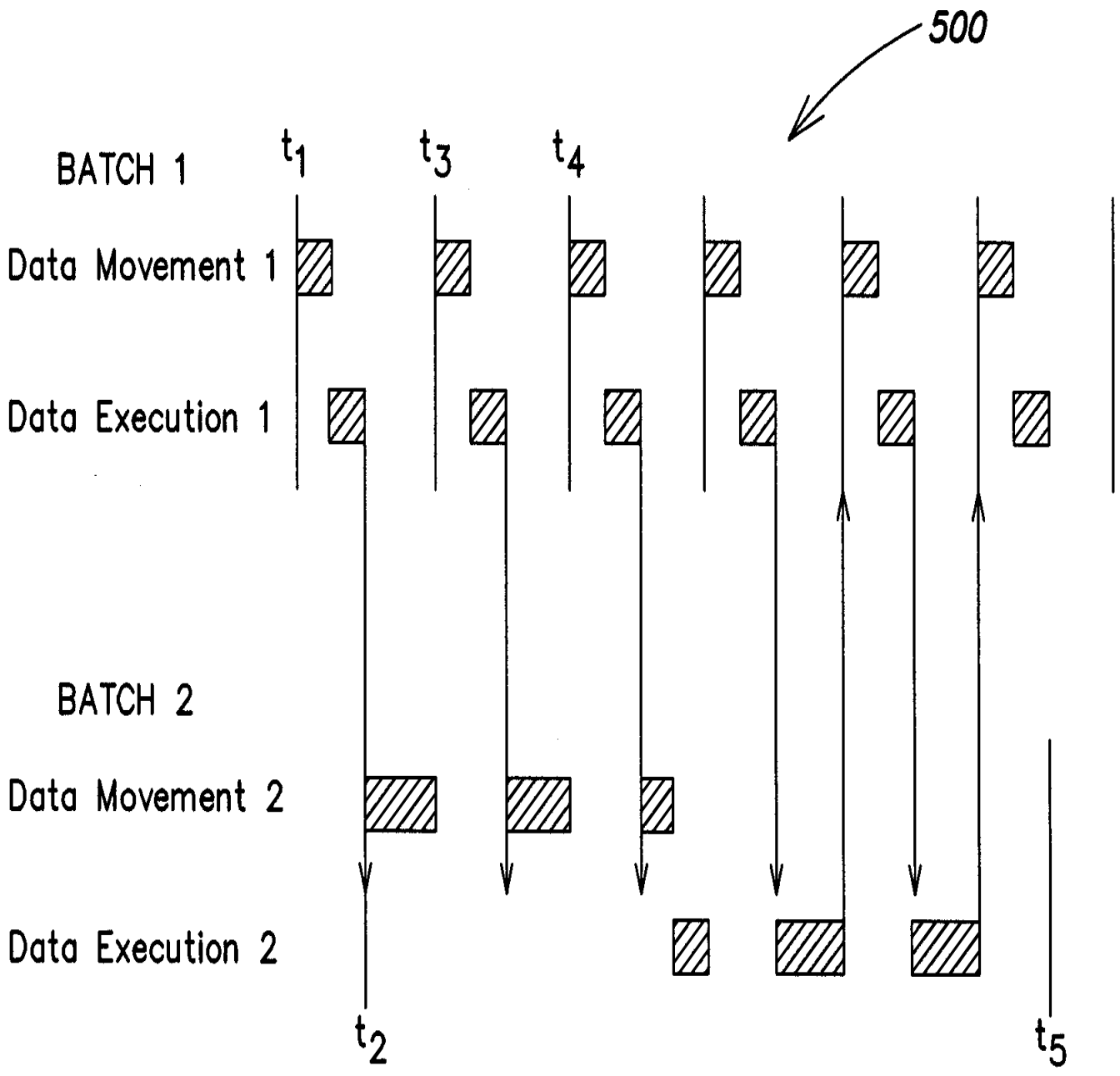
500
BATCH 1
t_1
t_3
t_4
Data Movement 1
Data Execution 1
BATCH 2
Data Movement 2
Data Execution 2
t_2
t_5

FIG. 5